

NOBLE HIGH-K DEVICE

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication and more specifically to formation of devices incorporating high-k dielectric gate oxide layers.

BACKGROUND OF THE INVENTION

High-k dielectric materials have been investigated to replace conventional gate oxide layers due to excellent current-leakage reduction seen when using the high-k dielectric materials at the same equivalent-oxide-thickness (EOT). However, high-k dielectric materials also suffer poor mobility and high threshold voltage issues in the electric performance of devices.

U.S. Patent No. 6,310,367 B1 to Yagishita et al. describes a strained Si and high-k gate dielectric Tx process wherein the concentration of Ge in the channel layer of the NMOSFET is lower than the concentration of Ge in the channel layer of the PMOSFET. The gate electrodes of the NMOSFET and the PMOSFET are made of metallic materials.

U.S. Patent No. 5,357,119 to Wang et al. describes an SiGe and gate oxide process.

U.S. Patent No. 6,353,249 B1 to Boyd et al. describes an SiGe substrate and high-k gate dielectric.

U.S. Patent Nos. 6,271,094 B1 to Chooi et al. and 6,335,238 B1 to Hanttangady et al. are related SiGe substrate and high-k dielectric Tx patents.

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U.S. Patent No. 6,287,903 B1 to Okuno et al. describes a structure and method for a large-permittivity dielectric using a germanium layer.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide improved substrate/high-k dielectric gate oxide material structures and methods of forming same.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having a strained substrate formed thereover is provided. The strained substrate comprising at least an uppermost strained-Si epi layer. At least one dielectric gate oxide portion over the strained substrate. The at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0. The at least one dielectric gate oxide portion being comprised of HfO_2 , HfSiO_4 , N-doped hafnium silicate (N-doped HfSiO_x), ZrO_2 or ZrSiO_x . A device over each of the at least one dielectric gate oxide portion to complete the least one high-k device. The invention also includes a method of forming the at least one high-k device.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Fig. 1 schematically illustrate a preferred embodiment of the present invention employing a first preferred embodiment strained-Si substrate.

Fig. 2 schematically illustrates a second preferred embodiment of the strained-Si substrate of the present invention.

Fig. 3 schematically illustrates a third preferred embodiment of the strained-Si substrate of the present invention.

Fig. 4 schematically illustrates a fourth preferred embodiment of the strained-Si substrate of the present invention.

Fig. 5 schematically illustrates a fifth preferred embodiment of the strained-Si substrate of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

For the purposes of this invention, all strained-Si epi layers/substrates have a dislocation density of strained-Si epi of less than about $1\text{E}6/\text{cm}^2$ and a high-k dielectric material has a dielectric constant (k) of greater than about 4.0.

Strained-Si Epi Layer 12 - Fig. 1 (First Embodiment)

As shown in Fig. 1, the preferred structure of the present embodiment includes a semiconductor structure 10 having a strained substrate 12 formed thereover to a thickness of preferably from about 3000 to 100,000Å and more preferably from about 4000 to 50,000Å.

In the first embodiment, strained substrate 12 is comprised of entirely of strained-silicon epitaxial (strained-Si epi). As noted above, strained-Si epi substrate 12 has a dislocation density of strained-Si epi of less than about $1\text{E}6/\text{cm}^2$.

Structure 10 is preferably a silicon substrate or a germanium substrate, is more preferably a silicon substrate and is understood to possibly include a semiconductor wafer or substrate.

Structure 10 may include: one or more NMOS areas 14 within which one or more NMOSFETs 18 (N-type metal-oxide semiconductor field effect

transistors) are formed; and may include one or more PMOS areas 16 within which one or more PMOSFETs 28 (P-type metal-oxide semiconductor field effect transistors) are formed. It is noted that a single, unitary strained-Si epi substrate layer 12 is formed under the NMOSFET's 18 and PMOSFET's 28 as this allows for enhanced mobility for both NMOS and PMOS devices 18, 28 and allows for a simpler process in forming the underlying strained substrate layer 12.

NMOSFET 18 and PMOSFET 28 each include respective high-k dielectric gate oxide portions 20, 30 that each have a thickness of preferably from about 10 to 200Å and more preferably from about 10 to 100Å. The respective high-k dielectric gate oxide portions 20, 30 each are preferably comprised of HfO_2 , HfSiO_4 , N-doped hafnium, HfSiO_x , ZrO_2 , ZrSiO_x or N-doped zirconium silicate (N-doped ZrSiO_x) and more preferably HfO_2 and HfSiO_4 . It is noted that respective high-k dielectric gate oxide portions 20, 30 are not formed of Ta_2O_5 , TiO_2 or Al_2O_3 as they have been found to have poor mobility, difficult process control and poor thermal stability. As noted above, high-k dielectric gate oxide portions 20, 30 have a dielectric constant (k) of greater than about 4.0.

Respective high-k dielectric gate oxide portions 20, 30 may be formed by depositing a layer of high-k dielectric gate oxide and then patterning it.

The high-k dielectric gate oxide portions 20, 30 have respective gate electrode portions 22, 32 having a thickness of preferably from about 500 to 2000Å and more preferably from about 700 to 1500Å and being preferably formed of

polysilicon (poly Si), TaN, WSi_x or tungsten (W) and more preferably polysilicon (poly Si) which is compatible with the current technology. It is noted that gate electrode portions 22, 32 are not metal gates, for example not TiN metal gates which, although having a lower work function, is hard to control even when employing dummy gates and has difficult integration issues.

Respective sidewall spacers 24, 34 are formed over NMOS and PMOS gate electrode portions 22, 32 to a maximum thickness of preferably from about 200 to 800Å and more preferably from about 250 to 600.

Respective source/drains 26, 36 are also formed adjacent NMOS and PMOS gate electrode portions 22, 32 within strained-Si epi substrate 12 to a maximum depth of preferably from about 300 to 1500Å and more preferably from about 400 to 1200Å.

As shown in Fig. 1, an isolation structure 40 may be formed within strained-Si epi substrate 12/structure 10 between NMOS/PMOS devices 18, 28 to electrically isolate them from each other for example. Isolation structure 40 may be a shallow trench isolation (STI) structure, for example.

It is noted that only NMOS devices 18, only PMOS devices 28 or other devices or a combination thereof may be formed over structure 10 and strained-Si epi substrate 12.

Strained-Si Epi Layer 54/Relaxed $\text{Si}_{1-x}\text{Ge}_x$ Layer 52/Graded $\text{Si}_{1-y}\text{Ge}_y$ Layer
Substrate 12 - Fig. 2 (Second Embodiment)

As shown in Fig. 2 and in the second embodiment, strained substrate 12 is comprised of an upper strained-Si epi layer 54 over a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 52 (where x is greater than 0 and less than about 0.50) which is in turn over a graded $\text{Si}_{1-y}\text{Ge}_y$ layer 50 (where y is 0 or about 0 proximate the interface between graded $\text{Si}_{1-y}\text{Ge}_y$ layer 50 which is in turn over a seed layer 41 and structure 10 and gradually increases (therefore graded) to about X at the interface between graded $\text{Si}_{1-y}\text{Ge}_y$ layer 50 and relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 52).

Upper strained-Si epi layer 54 has a thickness of preferably from about 100 to 500Å, more preferably from about 150 to 400Å and most preferably from about 200 to 300Å. Relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 52 has a thickness of preferably from about 1000 to 50,000Å. Graded $\text{Si}_{1-y}\text{Ge}_y$ layer 50 has a thickness of preferably from about 2000 to 50,000Å. Seed layer 41 has a thickness of preferably from about 10 to 200nm.

As noted above, strained-Si epi layer 54 has a dislocation density of strained-Si epi of less than about $1\text{E}6/\text{cm}^2$.

Strained-Si Epi Layer 62/SiO₂ Layer 60 (SOI Layer 12) - Fig. 3 (Third Embodiment)

As shown in Fig. 3 and in the third embodiment, strained substrate 12 is comprised of an upper strained-Si epi layer 62 over a Si_{1-x}Ge_x layer 61 which in turn is over a silicon oxide (SiO₂) layer 60 thus forming a silicon-on-insulator (SOI). Upper strained-Si epi layer 62 is bonded to SiO₂ layer 60.

Strained-Si epi layer 62 has a thickness of preferably from about 100 to 500Å, more preferably from about 150 to 400Å and most preferably from about 200 to 300Å. Si_{1-x}Ge_x layer 61 has a thickness of preferably from about 700 to 1200 Å. SiO₂ layer 60 has a thickness of preferably from about 800 to 2000Å.

As noted above, strained-Si epi layer 62 has a dislocation density of strained-Si epi of less than about 1E6/cm².

Strained-Si Epi Layer 78/Upper Relaxed Si_{1-x}Ge_x Layer 76/Graded Si_{1-y}Ge_y Layer 74/Thin Epi Layer 72/Lower Relaxed Si_{1-z}Ge_z Layer 70 - Fig. 4 (Fourth Embodiment)

As shown in Fig. 4 and in the fourth embodiment, strained substrate 12 is comprised of an upper strained-Si epi layer 78 over an upper relaxed Si_{1-x}Ge_x layer 76 (where x is greater than 0 and less than about 0.50 which is in turn over a graded Si_{1-y}Ge_y layer 74 (where y is about z proximate the interface between graded Si_{1-y}Ge_y layer 74 and epi layer 72 and gradually increases (therefore graded) to

about x at the interface between graded $\text{Si}_{1-y}\text{Ge}_y$ layer 74 and upper relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 77) which is in turn over a thin epi silicon layer 72 which is in turn over a lower relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer 70 (where z is greater than 0 and less than about y where $x \geq y \geq z$).

Upper strained-Si epi layer 78 has a thickness of preferably from about 100 to 500Å, more preferably from about 150 to 400Å and most preferably from about 200 to 300Å. Upper relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 76 has a thickness of preferably from about 1000 to 50,000Å and more preferably from about 2000 to 40,000Å. Graded $\text{Si}_{1-y}\text{Ge}_y$ layer 74 has a thickness of preferably from about 200 to 50,000Å and more preferably from about 500 to 25,000Å. Thin epi silicon layer 72 has a thickness of preferably from about 20 to 500Å and more preferably from about 50 to 200Å. Lower relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer 70 has a thickness of preferably from about 200 to 50,000Å and more preferably from about 500 to 25,000Å.

As noted above, strained-Si epi layer 78 has a dislocation density of strained-Si epi of less than about $1\text{E}6/\text{cm}^2$.

Upper Strained-Si epi layer 88/Relaxed- $\text{Si}_{1-x}\text{Ge}_x$ Layer 86/Constant $\text{Si}_{1-y}\text{Ge}_y$ Layer 84 /Si Epi Layer 82/Constant $\text{Si}_{1-z}\text{Ge}_z$ Layer 80 – Fig. 5 (Fifth Embodiment)

As shown in Fig. 5 and in the fifth embodiment, strained substrate 12 is comprised of an upper strained-Si epi layer 88 over an upper relaxed epi $\text{Si}_{1-x}\text{Ge}_x$ layer 86 (where x may be constant or graded) over constant (i.e. non-graded with a

constant Ge concentration $\text{Si}_{1-y}\text{Ge}_y$ layer 84 which is in turn over Si epi layer 82 which is in turn over constant $\text{Si}_{1-z}\text{Ge}_z$ layer 80 (i.e. non-graded with a constant Ge concentration); where $x \geq y \geq z$.

Upper strained-epi Si layer 88 has a thickness of preferably from about 20 to 500Å and more preferably from about 50 to 300Å. Upper relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer 86 (constant or graded) has a thickness of preferably from about 200 to 30,000Å and more preferably from about 300 to 5000Å. Constant $\text{Si}_{1-y}\text{Ge}_y$ layer 84 has a thickness of preferably from about 200 to 20,000Å and more preferably from about 300 to 5000Å. Si Epi Layer 82 has a thickness of preferably from about 20 to 500Å and more preferably from about 50 to 300Å. Constant $\text{Si}_{1-z}\text{Ge}_z$ layer 80 has a thickness of preferably from about 200 to 20,000Å and more preferably from about 300 to 5000Å.

Layers 80, 82, 84, 88 are strained layers.

NMOSFET(s) 18, PMOSFET(s) 28 and other devices formed over the high-k dielectric gate oxide portions 20, 30/strained substrate 12 may also be referred to as high-k devices as they incorporate high-k dielectric gate oxide portions.

Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. higher mobility of high-k devices is achieved; and
3. reduced threshold voltage of high-k devices is achieved.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.